DC Capacitor Voltages Balancing in Diode-Clamped Three-level Inverter-Based DSTATCOM

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Abstract

The Distribution Static Compensator (DSTATCOM) protects the utility transmission or distribution system from voltage sag and /or flicker caused by rapidly varying reactive current demand. Because of limitation of use of conventional two-level inverter based DSTATCOM in the field of high power applications, we used the multilevel inverter. This paper examines the application of a three level inverter based distribution static compensator (DSTATCOM) connected to distribution system. The multilevel inverter based DSATCOM has an inherent unbalancing problem among its dc capacitor voltages. Additionally, when the load contains a dc part, the neutral point of the compensator also becomes unbalanced. In this paper, the effects of different loading conditions on the dc capacitor voltages of the inverter are studied. Equations of the proposed equalizing controllers are developed corresponding to the control of the switching devices. Switching pulses for the three-level inverter are generated by Space Vector Modulation (SVM). Simulation results are provided to illustrate the performance of our controller. Validation of models and control algorithms is carried out through simulations in SimPower Systems of MATLAB/Simulink.

Keyword: DSTATCOM, Capacitor voltage equalization, Space Vector Modulation (SVM).

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I. INTRODUCTION

A Distribution Static Compensator (DSTATCOM) is an important shunt compensator which has the potential to solve many power quality problems faced by distribution systems [1].DSTATCOM is a custom power device connected in shunt with the distribution networks. It is used for reactive power compensation, voltage regulation, load balancing, harmonic filtering and power factor correction in distribution systems [2]. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage. For medium to high voltage applications and to meet the current and voltage harmonic distortion standards imposed on the line side, the recent trends are to use multilevel inverters to realize the shunt compensators in distribution systems[3][4]. There exist several types of multilevel inverters: cascaded Hibridge, diode clamped, flying capacitors . Less harmonic content, induces good power quality, lower switching losses, lower voltage distortion and eliminate the use of transformers are the important advantages of multilevel inverters [5].Among the multilevel VSI configurations, the diode-clamped multilevel inverter has been widely accepted for applications in high power drives and the utility systems [6]–[7]. Its main advantage is that the multilevel voltage outputs of the inverter are easily obtained with a low cost string of dc capacitors. In order to achieve different voltage levels, the inverters rely on split capacitor configurations.

Due to various reasons like unequal capacitance leakage currents, asymmetrical tracking of current, unequal delays in semiconductor devices, presence of dc components in the neutral current etc., the capacitor voltages drift away from the reference values, degrading the performance of the inverter. A number of techniques have been suggested to overcome this dc voltage imbalance problem like : 1) installing of voltage balancing circuits on the dc side of the converter [7]–[8] and 2) modifying the converter switching pattern according to a control strategy [9]–[10].

In this paper, the Space Vector Modulation (SVM) is used to generate three-level output and balance the voltages of DC-link capacitor, the proposed SVM scheme utilizes redundant switching states for the inverter voltage vectors which have unbalancing effect on the capacitor voltages. These switching states have opposite effects on the DC link capacitor voltages. Effective utilization of redundant switching states eliminates the need of extra hardware for the capacitor voltage balancing, without affecting the dwell timing of space vector over switching period.

The aim of the work is shows to implement the three-level inverter based DSTATCOM with control strategies in the MATLAB, Simulink using Simpower toolbox and to verify the results; various case studies applying different loads.

II. Three-Level NPC-Based DSTATCOM

The distribution static compensator is a power-electronic converter-based device used to regulate the grid voltage and control reactive power of the grid. In fact, the proposed DSTATCOM is a multilevel inverter connected to a grid in parallel at the point of common coupling (PCC). Fig. 1 shows a three-level NPC-based DSTATCOM configuration. The DSTATCOM is connected to a utility distribution system at a load terminal. The utility system is represented by a three-phase voltage source behind series RL elements in each phase. The load is a three-phase, passive RL load.

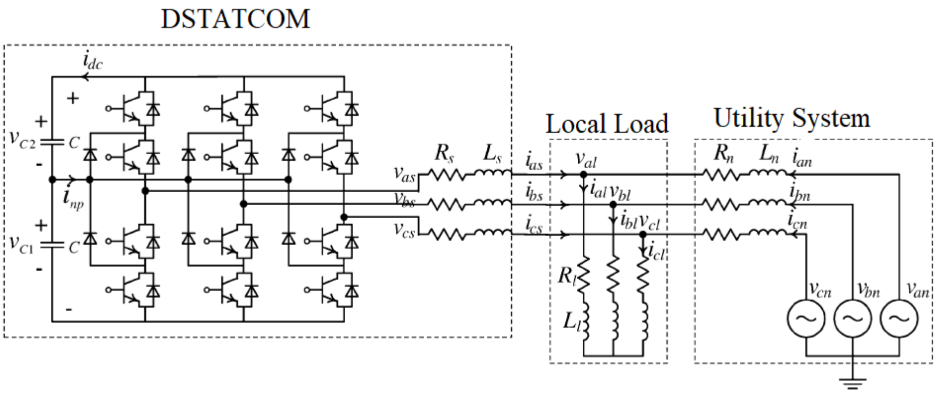


Fig. 1.Three-level NPC-based DSTATCOM connected to a utility system

If the output voltage of the VSC [20] and the source voltage are equal, no reactive power delivered to the system. When the output voltage of VSC is greater than the source voltage, the DSTATCOM [21] supplies reactive power to the grid, the DSTATCOM is in capacitive mode of operation. If the source voltage is greater than the output voltage of VSC, the DSTATCOM absorbs reactive power from the grid, the DSTATCOM is in inductive mode. The problem with two level converters based DSTATCOM [22] is the injecting unwanted harmonics in the power grid and is limited to operate at high frequencies due to switching losses, multilevel converters have the ability to resolve this issue.

III. Modeling of DSTATCOM

The modeling of DSTATCOM in state space is carried out in the synchronous reference frame method. Fig.1 shows the simplified single line diagram of a DSTATCOM. It consists of a DC link capacitor, three levels VSC, filter and point common coupling (PCC) as a voltage source. The relationships between the PCC voltage, inverter output voltages and currents are given by:

$$v_{as} = R_s i_{as} + L_s \frac{di_{as}}{dt} + v_{al}$$

$$v_{bs} = R_s i_{bs} + L_s \frac{di_{bs}}{dt} + v_{bl} \quad (1)$$

$$v_{cs} = R_s i_{cs} + L_s \frac{di_{cs}}{dt} + v_{cl}$$

These equations describe the system in differential equations in *ab*c frame. Transforming these equations to synchronous reference frame using Park's transformation results in:

$$v_{ds} = R_s i_{ds} + L_s \frac{di_{ds}}{dt} - L_s w i_q + v_{dl} \quad (2)$$

$$v_{qs} = R_s i_{qs} + L_s \frac{di_{qs}}{dt} + L_s w i_d + v_{ql} \quad (3)$$

The DC side current equation is given by:

$$I_c = -\frac{1}{v_{dc}}(v_{dl} i_{ds} + v_{ql} i_{qs}) \quad (4)$$

Since d-q axes are not stationary, they follow the trajectory of the voltage vector [10]. Within the synchronous rotating frame v=$v_{dl}$and v_{ql}=0 and hence the dc side current is given by:

$$I_c = -\frac{1}{v_{dc}} v_{dl} i_{ds} \quad (5)$$

The equations (2)-(3) and (5) describe the mathematical model of the DSTATCOM in the *dq* frame.

IV. DSTATCOM Control

A DSTATCOM is schematically depicted in Fig. 1. The VSC converts the voltage across the capacitor into a set of three-phase voltages. These voltages are in phase with the AC system and coupled with AC distribution system through the reactance of the coupling transformer. The DSTATCOM generates reactive power when system voltage is lower than its output voltage, and it said to be in capacitive mode. The DSTATCOM absorbs reactive power when system voltage is greater than its output voltage, and is said to be in the inductive mode. Insufficient reactive power in the system affects the bus voltage, which affect the sensitive loads connected to the bus. The equations (2) and (3) is a Multiple Input and Multiple Output (MIMO) system. The instantaneous voltage of the system and the DSTATCOM are independent, but the active and the reactive currents are coupled with each other through the reactance of the coupled inductor. So it is very essential to decouple the active and reactive current from each other and
design the controller for tracking the required value.

- ***Current Controller :***

The current controller design for the above system can be done using the strategy attempts to decouple the d and q axes equations, so that the MIMO system reduces to two independent Single Input Single Output (SISO) systems Hence, The control inputs $v_{ds}^*$and v_{qs}^*areconfigured as:

$$v_{ds} = v_d - L_s w i_q + v_{dl} \quad (6)$$

$$v_{qs} = v_q + L_s w i_d + v_{ql} \quad (7)$$

$$v_d = R_s i_{ds} + L_s \frac{di_{ds}}{dt} \quad (8)$$

$$v_q = R_s i_{qs} + L_s \frac{di_{qs}}{dt} \quad (9)$$

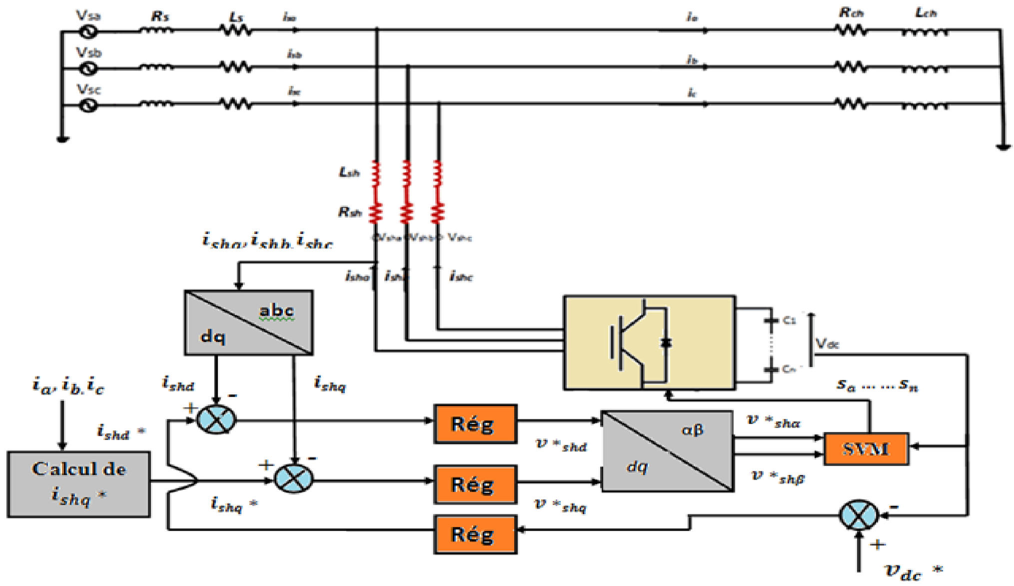


Fig. 2. Schematic of a DSTATCOM

From Equations (8) and (9) the two decoupling equation of the first order is defined :

$$\frac{di_{ds}}{dt} = \frac{1}{L_s} v_d - \frac{R_s}{L_s} i_{ds} \tag{10}$$

$$\frac{di_{qs}}{dt} = \frac{1}{L_s} v_q - \frac{R_s}{L_s} i_{qs} \tag{11}$$

The equations (10) and (11) are an independent SISO system. Conventional frequency-domain design methods can now be directly applied for current controller. The transfer function of a PI controller is:

$$G_i(s) = K_p + \frac{K_i}{s} \tag{12}$$

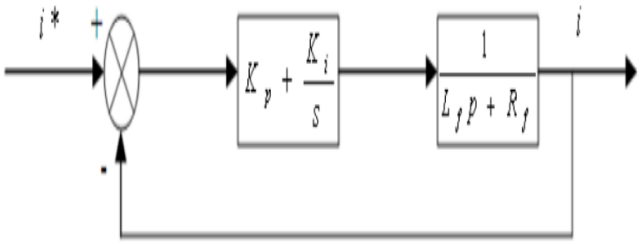


Fig. 3. Effective closed loop current control system

The closed loop transfer function of this system is:

$$H_i(s) = \frac{k_{pi}s + k_{ii}}{L_f s^2 + (R_f + k_{pi})s + k_{ii}} \tag{13}$$

Then the system behaves as second order, so the parameters of PI controller are defined as:

$$\begin{cases} k_{pi} = 2\varepsilon w_i L_f - R_f \\ k_{ii} = L_f w_i^2 \end{cases} \tag{14}$$

- ***DC voltage Controller***

The relation between dc current $i_{dc}$and dc voltage$v_{dc}$is:

$$i_c = C\frac{dv_{dc}}{dt} \tag{15}$$

The transfer function can be written as:

$$G_v(s) = \frac{1}{Cs} \tag{16}$$

The closed loop transfer function can be written as:

$$H_v(s) = \frac{k_{pv}s + k_{iv}}{Cs^2 + k_{pv}s + k_{iv}} \tag{17}$$

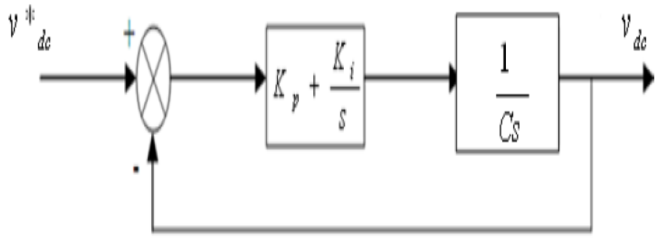


Fig. 4. DC link voltage control loop

The parameters of PI controller are defined as:

$$\begin{cases} k_{pv} = 2\varepsilon w_v C \\ k_{iv} = C w_v^2 \end{cases} \tag{18}$$

Space Vector Modulation Strategy.

- ***Switching States :***

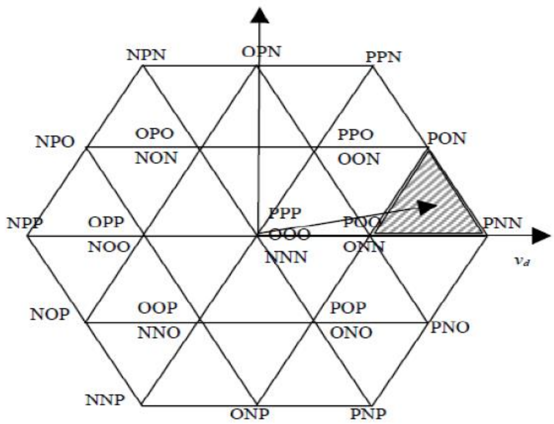


Fig. ***5***. Hexagon showing voltage vectors of3-level inverter

Each phase of the three level diode clamping inverter consists of four switching devices and two clamping diodes. The DC supply consists of two capacities in series. Table 1 shows the switching states of each phase of the inverter. Since three kinds of switching states exist in each phase, the three levels inverter has 3^3 = 27 switching states. Fig.5 shows the space vector representation of the output voltage.

vectors are identified as PON, PNN, etc. For example, in the case of PON, the output terminals U,V, and W have the potentials E, 0, and –E respectively. There are 27 vectors in this space vector diagram, which are divided into 4 groups according to its amplitude: large vectors (e.g. PNN), medium vectors (e.g. PON), small vectors (e.g. POO) and zero vectors (e.g. NNN). Small and zero vectors are redundant, while large and medium vectors are not.

TABLE I. STATES OF THREE LEVEL INVERTER

Switching Symbols	Switching States				Output Voltage
P	On	On	Off	Off	E
O	Off	On	On	Off	0
N	Off	Off	On	On	-E

B. Voltage Vector Synthesis :

In this paper, switching for the inverter of DSTATCOM are generated by Space Vector Modulation (SVM) technique. SVM method [18] is an advanced computation intensive PWM [19] technique and the literature says that it is the best among all PWM techniques for digital implementation in variable frequency drive application [11].

The SVM strategy is proposed in [12]. It consists of the generation of a specific sequence of states of the inverter. The reference voltage vector is defined as:

$$V^* = v_a^*.e^{j0} + v_b^*.e^{-j2\pi/3} + v_c^* e^{j2\pi/3} = v_d^* + jv_q^* \qquad (19)$$

V_d^* and $v_q^*$are the components of the vector V^* in the plan d-q. This vector takes eighteendiscrete positions in dq plane according to the status of the inverter.These positions are shown on the vector diagram of the inverter (Fig. 5). They are arranged on two hexagons: twelve positions on the outer hexagon (corresponding to states PNN, PON,PPN, OPN, NPN, NPO, NPP, NOP, NNP, ONP, PNP and PNO), six on the internal hexagon (Corresponding to the states (POO-ONN) (PPO-OON) (OPO-NO) (OPP-NOO)(OOP-NOS) and (POP-ONO)), in more than one position at the origin of the diagram, corresponding to the states PPP, OOO and NNN.

C. Determination of region and sector:

From the coordinates $v^*{}_d$and $v^*{}_q$and the angular position *θ*, we deduce in what area (*s*), and what region (*r*) is the vector v^* situ in the *dq* plane. The triangular area is derived as follows:

$$S = \begin{cases} 1 & if \quad 0 \le \theta < \pi/3 \\ 2 & if \quad \pi/3 \le \theta < 2\pi/3 \\ 3 & if \quad 2\pi/3 \le \theta < 3\pi/3 \\ 4 & if \quad 3\pi/3 \le \theta < 4\pi/3 \\ 5 & if \quad 4\pi/3 \le \theta < 5\pi/3 \\ 6 & if \quad 5\pi/3 \le \theta < 2\pi \end{cases} \qquad (20)$$

The triangular region within each sector is inferred using the equations of its three sides. The switching times T_x, T_y, T_z for any sector is given in Table II.

TABLE I. SWITCHING TIME DURATION AT ANY SECTOR

	T_x	T_y
Region 1	$2T_s.m.\sin(\pi/3-\alpha)$	$2T_s.m.\sin(\alpha)$
Region 2	$T_s(1-2m.\sin(\pi/3-\alpha))$	$T_s(1-2m.\sin\alpha)$
Region 3	$T_s(2m.\sin(\pi/3-\alpha)-1)$	$2T_s\ .m.\sin\alpha$
Region 4	$T_s(2m.\sin(\pi/3-\alpha)-1)$	$T_s(2m.\sin(\alpha)-1)$
For all regions: $T_z = T_s - T_x - T_y$		

αis : The angular position of vector V^* within a sector: $a = \theta\ [\pi\ /\ 3]$.

V. Neutral Point Voltage Control

Different techniques to balance the voltages on the dc- link capacitors have been reported in the literature for the conventional three-level, three-leg NPC converter. These are usually categorised as active control, passive control and hys-teresis control. [13], [14], [15]. In this work an active control methodology, embedded into the utilisation and selection of the SVM redundant vectors, is proposed to balance the capacitor voltages. In the space vector diagram of three-level inverter (Fig. 5), we can distinguish four types of vectors: large vectors (PNN, PPN, NPN, NPP, NNP and PNP), mediumvectors (PON, OPN,NPO, NOP,ONP and PNO), small vectors (PPO, OON, OPO, NON, OPP, NOO, OOP, NNO, POP,ONO, POO and ONN) and zero vectors (PPP, OOO and NNN). Table 5 shows the currents injected by all small and medium vectors [16]. As we see, each small redundant vector can inject either positive or negative current. Those small vectorsinjecting positive phase currents into the neutral point will be called positive vectors (ONN, PPO, NON, OPP, NNO, POP), while those injecting opposite phase currents will be called negatives vectors (POO, OON, OPO, NOO, OOP, ONO).
Medium vectors also affect ne utral point potential. However, as they are not redundant vectors, this influence will not be controlled, being ther efore considered as perturbation for the dc-voltage stabilization [17].

TABLE II: NEUTRAL POINT CURRENT FOR DIFFERENT SPACE VECTORS

Positive Small vectors	I_{NP}	Negative Small vectors	I_{NP}	Medium vectors	I_{NP}
ONN	i_a	POO	$-i_a$	PON	i_b
PPO	i_c	OON	$-i_c$	OPN	i_a
NON	i_b	OPO	$-i_b$	NPO	i_c
OPP	i_a	NOO	$-i_a$	NOP	i_b
NNO	i_c	OOP	$-i_c$	ONP	i_a
POP	i_b	ONO	$-i_b$	PNO	i_c

Fig. 6. show the effect of the two small vectors with two different switching combinations: (POO) and (ONN) on the neutral point potential.These two vectors produce the same output voltage, but when the vector POO is applied, the current flows into theneutral point ($i_{NP} = -i_a$),while with the vector ONN, the current flows out ($i_{NP} = i_a$).

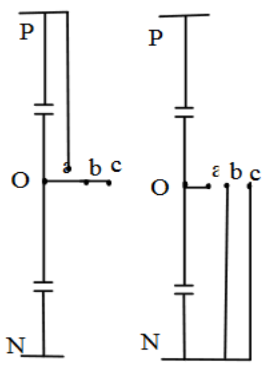


Fig.6 Neutral point connections

The neutral point potential control is based on the use of both two redundant vectors in each sector, in order to inject positive or negative current in neutral point, depending on the value of the voltages of the two capacitors V_{dc1} and V_{dc2} , and the load current:

If we have $V_{dc1}>V_{dc2}$, in order to make $V_{dc1}=V_{dc2}$ we must inject a current either from O to P in order to reduce V_{dc1} , or from O to N in order to increase V_{dc2} . In both two cases, we have $i_{NP}< 0$.

If we have $V_{dc1}<V_{dc2}$, in order to make $V_{dc1}=V_{dc2}$, we must increase V_{dc1} by injecting a current from P to O, or decrease V_{dc2} by injecting a current from N to O. In both two cases, we have $i_{NP}>0$.

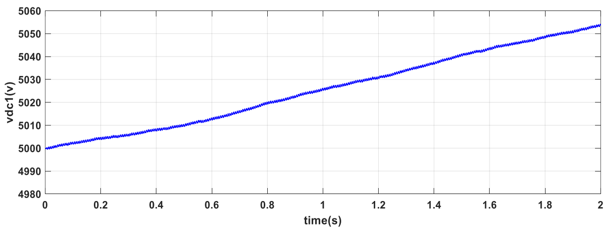
Therefore, for insure the neutral point potential control we have to ensure the following relationship between V_{dc1} , V_{dc2} and i_{NP}:

$$(V_{dc1} - V_{dc2}).\, i_{NP} \leq 0 \tag{21}$$

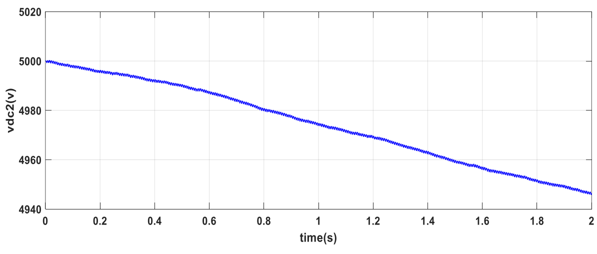
In the control scheme of the neutral point potential we make a continuous measurement of the two dc-voltages V_{dc1} and V_{dc2} and the neutral point current i_{NP} given by equation (21). We calculate the product (V_{dc1}-V_{dc2}). i_{NP}. If this product is negative we kept the set of small vectors (positive or negative one) used in the previous sample of time. Otherwise we must change this set of small vectors in the previous sample of time in or der to inverse the sense of the neutral point current i_{NP}.

VI. Simulation Results

In this study, the model of power system, DSTATCOM and controller are developed in MATLAB/Simulink environment. PI controllers were used for controlling DSTATCOM. The performance of DSTATCOM is studied in a power system. The distribution part of the power system is represented by a The venin's equivalent voltage source and short circuit impedance. The operation of the DSTATCOM device in a electric power transmission line will be validated in the two modes of capacitive and inductive compensation. Initially the DC bus capacitor is charged and the voltage across the latter is 10 kV. At the beginning of the simulation, the grid supplies the load (L1). The second charge (L2) is connected to the grid at time (t = 0.25s), and at time (t = 0.5s) line is loaded by load (L3), and finally at time (t = 0.75s) both load (L1) and (L2) is Logged Out. Fig. 6 show the two dc-voltages without the balancing algorithm. The performance of DC-link voltage balancing control schemes are show in Fig.7, this result prove the efficiency of the given control scheme which is simple but powerful. The capacitor voltage is maintained at 10 kV as shown in Fig.8. Fig. 9. shows the dynamics of reactive current exchanged between the DSTATCOM and network, initially the electrical source feeds an inductive load therefore the reactive current is negative and the DSTATCOM operate in inductive mode (DSTATCOM delivers reactive power), when we charge the network by the capacitive load the reactive current becomes positive and the DSTATCOM Operate in capacitive mode (DSTATCOM absorbs reactive power). The active current exchanged between the DSTATCOM and network as shown in Figure 10.

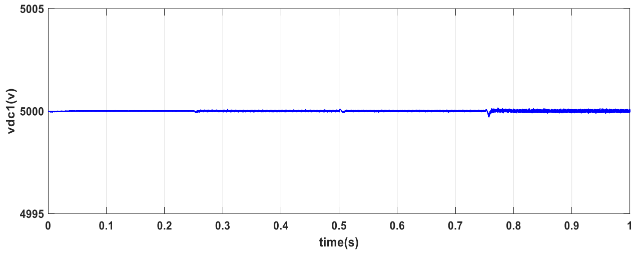


(a)

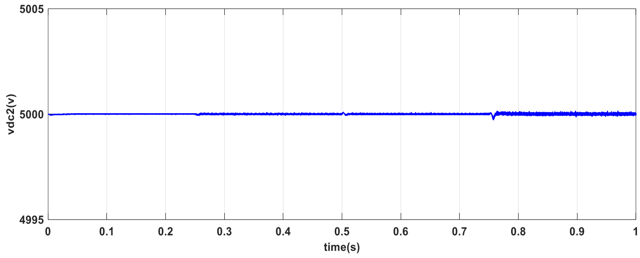


(b)

Fig. 6. Dc link capacitors voltage without balancing



(a)



(b)

Fig. 7. Dc link capacitors voltage with balancing

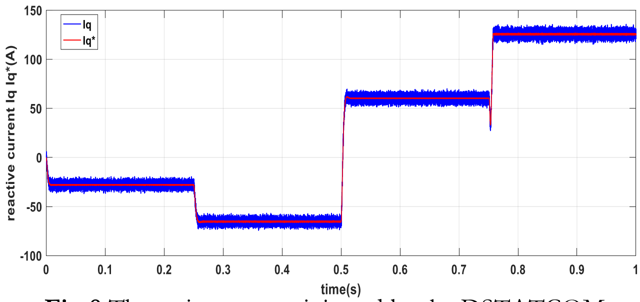


Fig.8 The active current injected by the DSTATCOM

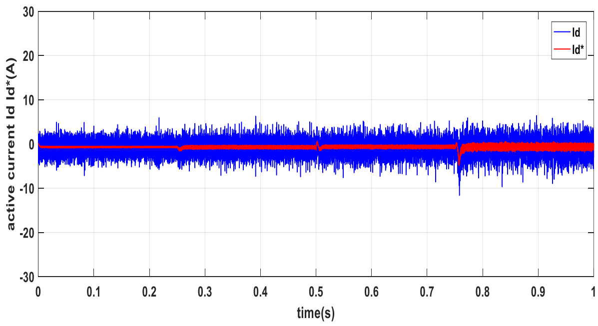


Fig. 9. The reactive current injected by the DSTATCOM

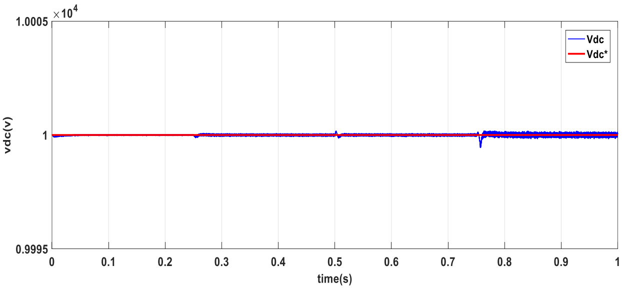


Fig.10. The active current injected by the DSTATCOM

VII. Conclusion

In this paper, a DSTATCOM based three-level inverter in order to improve the power quality is studied. PI controller is proposed for the control of DSTATCOM, with the aim of improving the quality of electric power, and corrects the power factor. The space vector modulation technique is used for three-level inverter. The main feature of the SVM strategy is that it can balance the dc capacitor voltages without the need for corrective control action or auxiliary devices. The study results show the effectiveness of the selected switching strategy in balancing dc capacitor voltages under various system operating conditions, and the effectiveness of the method adopted in the regulation of active and reactive power through the control of active and reactive currents.

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