Continuous-Time Sigma-Delta Modulator Circuit Design Using 130nm CMOS Technology

Abdelghani Dendouga[1], Brahim Lakehal[2]

[1]Dept. of Electronic, University of Batna 2, Advanced Electronics Laboratory of University of Batna 2 (Algeria).

[2]Institute of Hygiene and Industrial Security, University of Batna2 (Algeria).

The Author's E-mail: a.dendouga@univ-batna2.dz[1], b.lakehal@univ-batna2.dz[2]

Recieved: 22/11/2023 Accepted: 12/03/2024 Published: 25/03/2024

Abstract

This paper presents a detailed study on the design and implementation of a continuous-time Sigma- Delta (ΣΔ) modulator. The objective of this research is to achieve high-precision analog-to-digital conversion with improved performance in terms of resolution and noise shaping capabilities. The modulator is designed using a two-stage architecture for the operational amplifier (Op-Amp) to enhance power efficiency and space utilization. The paper outlines the design methodology, which involves circuit analysis, component selection, and simulation to optimize the modulator's performance. Various performance metrics are considered, including resolution, signal-to-noise ratio (SNR), distortion, and dynamic range. The designed continuous-time Sigma-Delta modulator is implemented using advanced electronic design automation (EDA) tools, and the performance is evaluated through extensive simulations. The simulations are conducted utilizing standard CMOS technology, and the modulator's behavior is analyzed under different operating conditions.

Keywords: - CMOS analog circuit design, Sigma delta modulators, Analog to digital converters, Operational amplifier.

Tob Regul Sci.™ 2024;10(1):1823 - 1833

DOI: doi.org/10.18001/TRS.10.1.115

Introduction

In recent years, the demand for high-performance data conversion has grown exponentially across variousapplications, including wireless communications, multimedia, sensor networks, and digital signal processing. Among the different types of analog-to-digital converters (ADCs), sigma-delta modulators have gained significant attention due to their ability to achieve exceptional resolution and noise shaping capabilities. In particular, continuous-time sigma-delta modulators have shown promising performance advantages, making them an attractive choice for data acquisition systems requiring high precision and robustness against noise [1, 2].

The objective of this paper is to present a comprehensive study and design of a continuous-time sigma- delta modulator. Continuous-time sigma-delta modulators are known for their suitability in high-frequency applications and their potential for integration with advanced CMOS

technologies, allowing for the realization of compact and power-efficient designs.

This research delves into the intricacies of continuous-time sigma-delta modulators, exploring their principles of operation, architecture, and key parameters affecting their performance. By understanding the theoretical underpinnings, we aim to optimize the modulator's behavior and tailor it to meet the requirementsof specific applications [3-5].

Moreover, this paper addresses the challenges faced during the design process, including non-idealities, stability, and linearity issues that might affect the modulator's overall performance. By systematically

analyzing these challenges and proposing effective solutions, we strive to enhance the modulator's robustness and reliability [6].

The design and simulation of the continuous-time sigma-delta modulator will be carried out using advanced electronic design automation (EDA) tools, and the performance will be evaluated using state-of- the-art simulation techniques. Emphasis will be placed on achieving a balance between high-resolution data conversion and power efficiency, as power consumption remains a critical consideration in many portable and energy-constrained applications.

The contributions of this paper are twofold: First, we present a comprehensive survey of the existing literature on continuous-time sigma-delta modulators, outlining their strengths and limitations. Second, we propose a novel architecture and design optimization techniques to push the boundaries of performance while addressing the design challenges associated with these modulators.

In conclusion, this paper aims to advance the state-of-the-art in continuous-time sigma-delta modulator design and contribute valuable insights to the field of high-performance data conversion. The research presented here serves as a solid foundation for the development of robust and efficient continuous-time sigma-delta modulators, with the potential to revolutionize various applications requiring accurate and reliable analog-to-digital conversion.

Continuous time Sigma Delta ADC

The sigma-delta ADC concept has been extensively explored in prior works [9,10]. Figure 1 presents a simplified block diagram of the ADC, comprising components such as an integrator (capacitor), a comparator, two voltage-to-current converters, and an analog switch 'S,' controlled by the comparator's output and a clock-triggered flip-flop 'clk.' The input voltage signal is transformed into a current 'IIN,' which charges the capacitor 'C.' Once the voltage across the capacitor reaches the V_{ref} level, the capacitor is discharged through the switch 'S' with a current of 'I_{Ref}.' As a result, a clock-synchronized triangular waveform is generated (Figure 1), wherein the difference in the number of up and down pulses represents the ratio between the input voltage and the reference voltage [7-11].

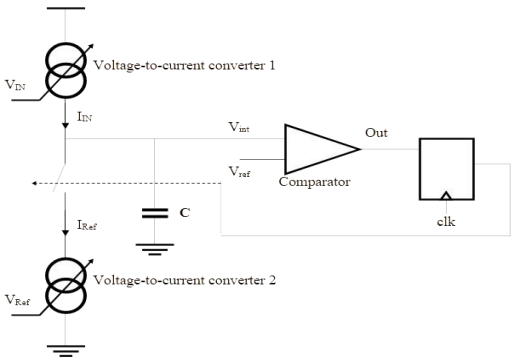

Fig. 1. Continuous time sigma delta ADC

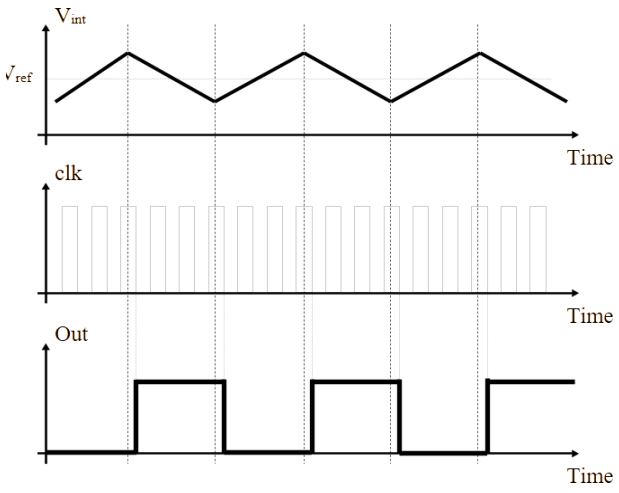

Fig. 2. Continuous time sigma delta ADC (wave plot)

To ensure high linearity of the ADC across varying temperatures and voltage supplies, two identical voltage-to-current converters are employed, guaranteeing a precise match between the charge and discharge currents Figure 2. This design approach facilitates a relatively straightforward silicon implementation, reducing space requirements and power consumption. The ADC is specifically tailored for measuring signals from pressure and/or temperature sensors in industrial applications, and accordingly, the design requirements are pre-established to cater to the characteristics of these sensors. For a quick reference, Table 1 provides an overview of the main design requirements.

Table 1. Design performances requirement

Parameters	Typ	Unit
Frequency	2	MHz
Voltage supply	1.8	V
Temperature range	27	°C
Resolution	10	Bit
Integral non-linearity error	<1/2	LSB
Differential non-linearity error	<1/2	LSB
Current consummation “estimation”	300	µA

Circuit-level implementation The operational amplifier

The operational amplifier (Op-Amp) plays a crucial role as the central component within a sigma-delta

modulator (SDM). The performance of the sigma-delta converter, encompassing its resolution and speed, is primarily governed by the Op-Amps employed in the SDM. The precision of the Op-Amp's output is limited by its open-loop DC-gain, while its bandwidth and slew rate establish the maximum clock frequency it can support. To achieve an optimized signal-to-noise ratio, the Op-Amp should offer a wide output signal swing.

The Op-Amp's characteristics, specifically its DC-gain within the SDM, are influenced by the resolution, whereas the slew rate and Gain Bandwidth Product (GBW) specifications can be determined based on the analog-to-digital converter's sampling speed. In a sigma-delta ADC, the sampling speed relies on the amplifier's settling time in the SDM, with the slew rate primarily impacting this aspect and the gain bandwidth playing a decisive role in the final design.

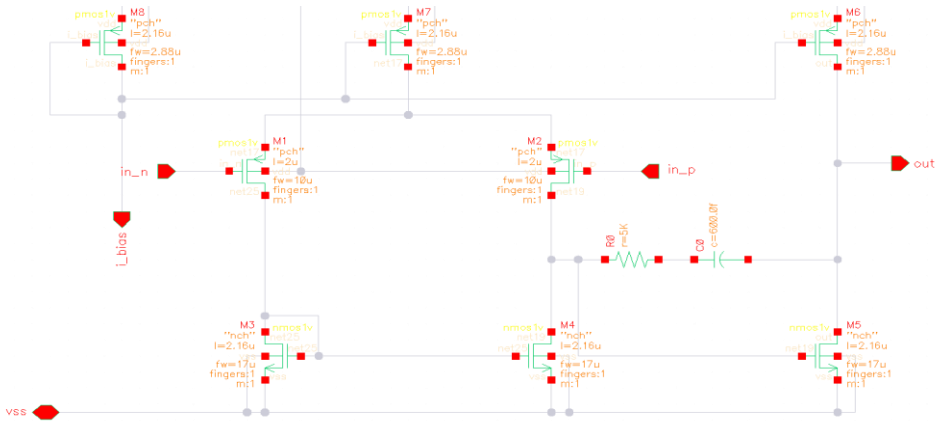

Fig. 3. The AOP schematic

We have opted for a straightforward two-stage architecture for the operational amplifier, utilizing an operational transconductance amplifier (OTA). The decision to use the OTA was motivated by its advantageous features, including a high voltage gain and a superior output resistance.

The OTA configuration comprises an input differential stage, consisting of transistors M1 and M2, which are biased by a current mirror composed of M3 and M4. The output stage is constructed using an NMOS amplifier stage, employing transistors M5 and M6, and it is biased by transistor M8. By introducingcapacitors and resistors, we can incorporate amplifier compensation to fine-tune its phase margin.

Our specific goal is to design a Miller OTA with the following targeted characteristics:

- Av > 60 dB, 20.log (2N-1) where N is the resolution of our converter (10 bits).
- GBW ≥ 10 MHz, 10 MHz being the operating speed of our converter.
- Pm ≥ 67° to ensure amplifier stability.Av: open-loop gain

GBW: bandwidthPm: phase margin

Table 2. the designed AOP performances

Performance	Specification	Spectre	Unit
DC gain	≥70	89.15	dB
Unity Gain Bandwidth	≥10	47.69	MHz
Phase Margin	≥60	64	deg
Slew Rate	Max	2.19	V/µs
Area	Min	-	µm2
Power	Min	0.051	mW
Technology	TSMC 130	-	nm

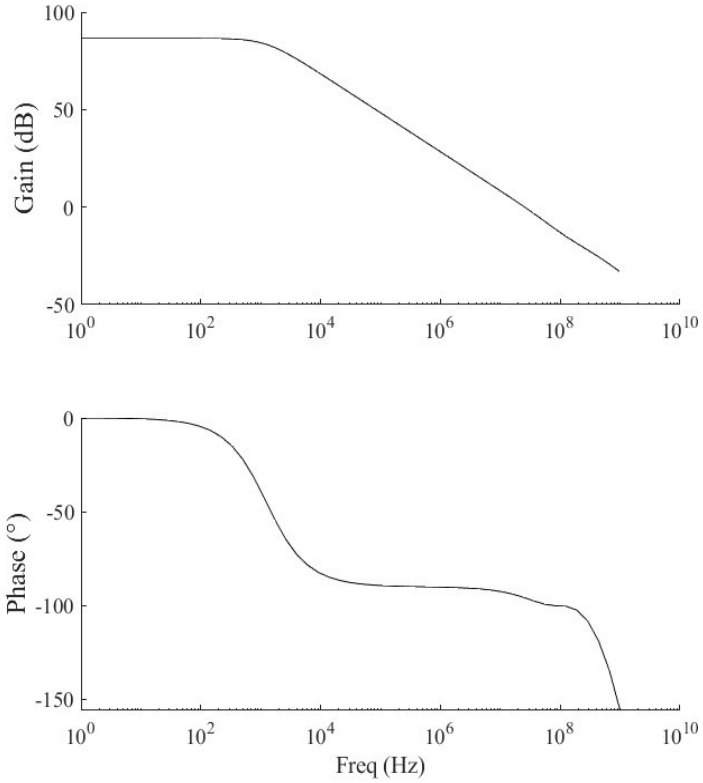

Fig. 4. Bode diagram of the designed operational amplifier

Voltage to current converter

To achieve an output current that is directly proportional to the input voltage, the voltage-to-current converter circuit heavily depends on the amplifier's performance. Therefore, careful selection of the amplifier's architecture is crucial. To create an efficient voltage-to-current converter, a current mirror is essential [12].

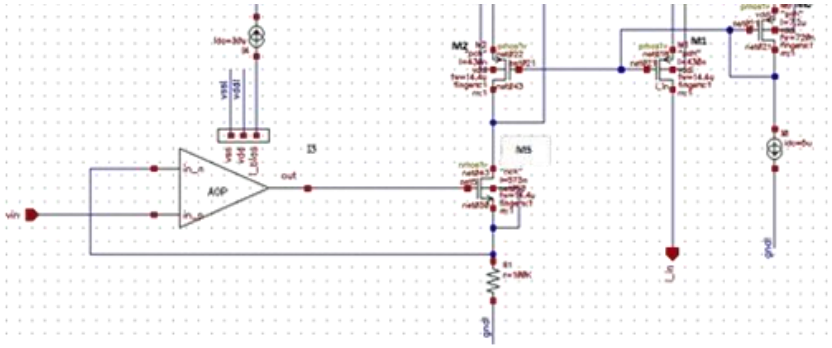

Fig. 5. Schematic of the voltage to current converter

This improved mirror circuit configuration ensures a more stable current source or sink, resulting in a more accurate input for the output current gain. The current mirror is integrated alongside the operational amplifier in our voltage-to-current converter, as shown in Figure 5, depicting the converter's structure.

Comparator

A comparator is a component that, for a given voltage difference between its two inputs, outputs

a logic voltage equal to "1" or "0."

The simplified electrical diagram of a dynamic comparator is illustrated in Figure 6.

The comparator operates as follows: When the "clk" signal is at the low state (0 V), transistors M6 and M9 are active. The outputs "out_1" and "out_2" are at the high state (VDD). Additionally, transistor M3 is in the off state, and the comparator is in its idle phase. At the rising edge of "clk," M3 enters its active region, and transistors M6 and M9 turn off. An imbalance occurs in the latch formed by transistors M5-M7 and M4-M8, resulting in one of the two outputs switching depending on the state of the input signal (in_1) with respect to the reference thresholds (in_2).

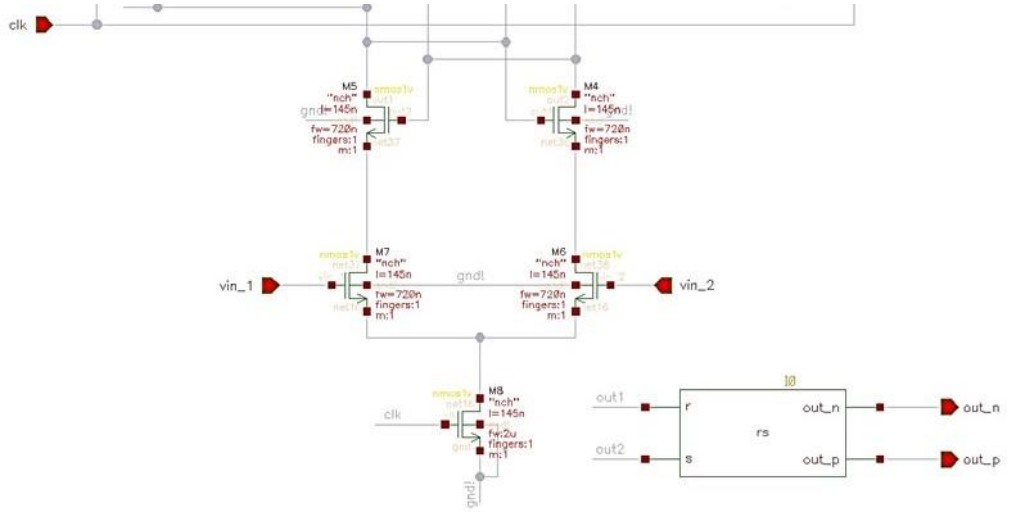

Fig. 6. Comparator schematic

The comparator operates as follows: When the "clk" signal is at the low state (0 V), transistors M6 and M9 are active. The outputs "out_1" and "out_2" are at the high state (VDD). Additionally, transistor M3 is in the off state, and the comparator is in its idle phase. At the rising edge of "clk," M3 enters its active region, and transistors M6 and M9 turn off. An imbalance occurs in the latch formed by transistors M5-M7 and M4-M8, resulting in one of the two outputs switching depending on the state of the input signal (in_1) with respect to the reference thresholds (in_2).

Simulation results

Having concluded the design of the distinct fundamental blocks, we are now prepared to advance towards the implementation of the complete circuit for our comprehensive Sigma-Delta modulator. The ensuing figure provides an illustration of the entire schematic.

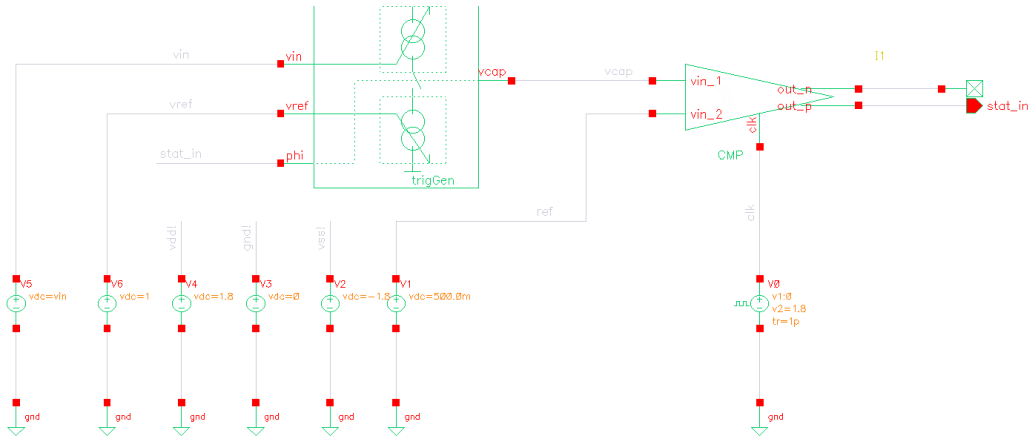

Fig. 7. The sigma delta modulator test bench

The simulations will be conducted using a supply voltage of 1.8V, and various input voltage values, specifically Vin at 100mV, 500mV, and 900mV. The system clock period will be fixed at 100 ns, and the reference voltage Vref will be set to 500mV. The transient simulation will encompass a duration of 5µs.

The primary objective of these simulations is to analyze and evaluate the influence of the input signal Vin on both the triangular waveform at the capacitor terminals Vcap and the output signal of the comparator Vstat_in.

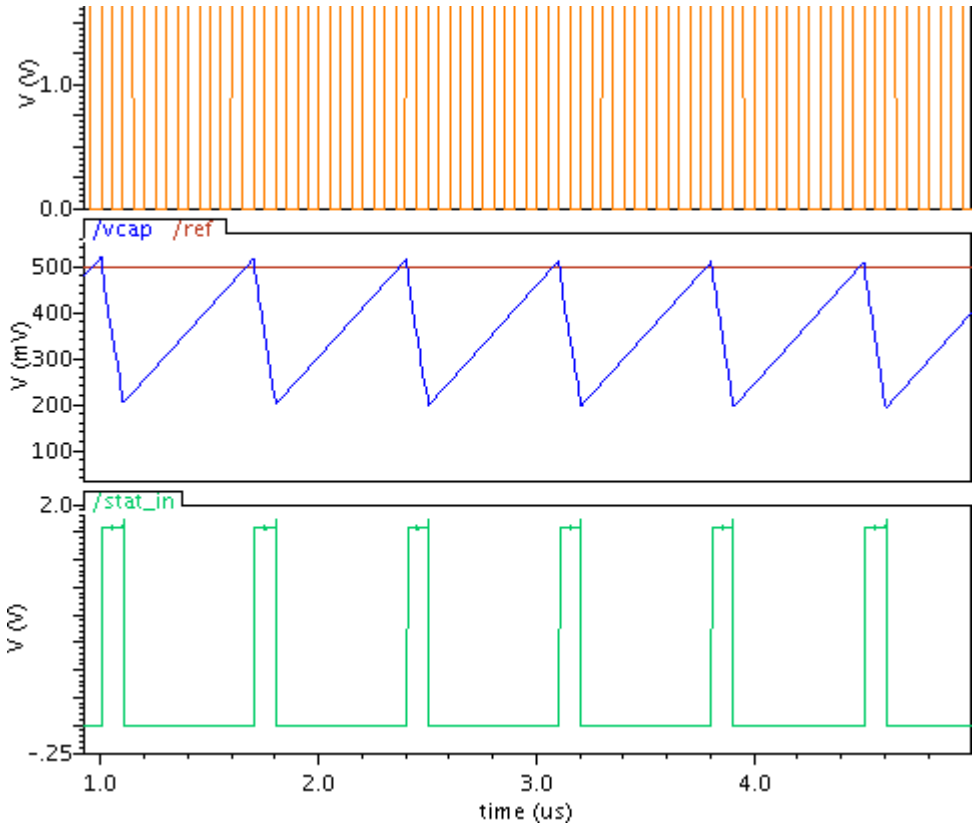

Fig. 8. Transient simulation results of the modulator for input voltage equal to 100mV.

In a simplified explanation, the accumulation of the 1-bit flux (bitstream) over N clock cycles results in adecimated value. This value represents the average of the bitstream output from the modulator, as illustrated

in Figure 8. Subsequently, the obtained bitstream undergoes digital filtering to achieve an N-bit representation of the analog input, as demonstrated in Figure 8.

By employing interpolation of the transfer function, we can ascertain the trend curve, represented by the function y = 1014x + 10.31, as illustrated in Figure 9. Utilizing this trend curve, we proceed to calculate the converter's value for each input voltage in the ideal scenario.

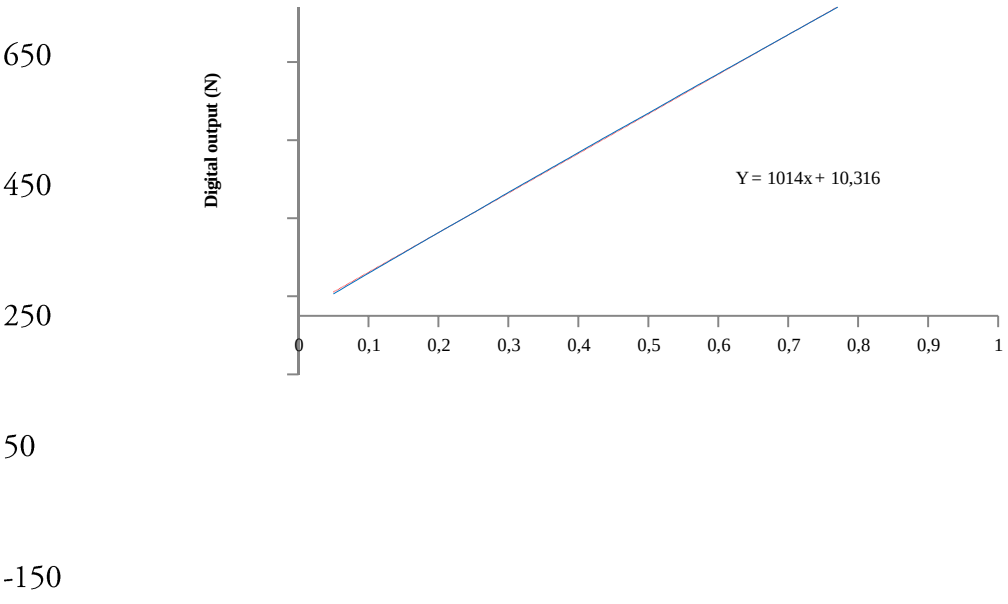

Fig. 9. Transfer function of the sigma delta modulator and its best fited line.

The discrepancy between the acquired code and the value computed using the curve-fitting function signifies the conversion error (Figure 10).

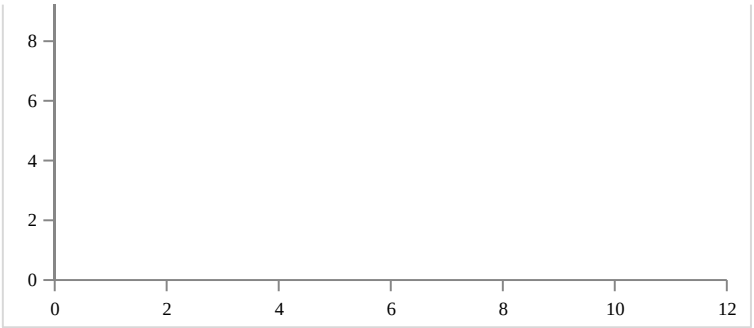

Fig. 10.The error curve

Conclusion

The primary aim of this research was to conduct a thorough investigation and develop analog-to-digital converters based on a Sigma-Delta modulator architecture. This modulator design ensures efficient power utilization and high conversion accuracy, offering a resolution of 10 bits.

Various system components were meticulously examined and designed, encompassing:

- A diverse set of standard cells, including inverters, NAND gates, buffers, and RS flip-flops.

- An essential operational amplifier, pivotal to the system, featuring an open-loop gain of 89.15 dB and a gain bandwidth of 47.69 MHz. It plays a crucial role in facilitating the proper operation of the integrator circuit and is also employed as a summing circuit, providing the differential feedback input to the integrator.

- Two voltage-to-current converters responsible for delivering constant currents, which correspond to the input voltage and reference voltage, respectively.

- A high-speed comparator employing a dynamic comparator approach to compare the input signal with a reference signal and subsequently deliver the output corresponding to the voltage converter.

Following an exhaustive analysis, the modulator's functionality was verified through comprehensive simulations. The Sigma-Delta modulator was designed and simulated utilizing the CADENCE environment, with the implementation based on the 130nm technology of TSMC (Taiwan Semiconductor Manufacturing Company).

References

[1] Swamy, M. N. S., & Chandrakasan, A. P, “Continuous-Time Sigma-Delta Modulators: A Review”, IEEE Signal Processing Magazine, (2002),19(4), 66-84.

[2] A. Dendouga, M.L. Hafiane, N. Bouguechal, S. Oussalah, S. Barra, S. Kouda, “Analog design- for-testability technique for first-order sigma delta ADC”, Measurement, (2013),46(9), 3342- 3346.

[3] Wang, S., Zhang, W., & Chen, G, “A Low-Power Continuous-Time ΣΔ Modulator with Improved Noise Shaping”, IEEE Journal of Solid-State Circuits, (2010), 45(1), 135-143.

[4] Chen, Y., Wang, X., & Wang, Y, “A High-Performance Continuous-Time ΣΔ Modulator for Biomedical Applications”, IEEE Transactions on Biomedical Circuits and Systems, (2012), 6(2), 145-153.

[5] Zhang, R., Zhang, W., & Wang, S, “A Continuous-Time ΣΔ Modulator with Improved Resolution and Dynamic Range”, IEEE Transactions on Circuits and Systems I, (2014), 61(12), 3234-3243.

[6] Lu, J., Zhang, J., & Wang, Y, “A Continuous-Time ΣΔ Modulator with Reduced Sensitivity to Non-Idealities”, IEEE Transactions on Circuits and Systems I, (2016), 63(10), 2629-2639.

[7] Zhang, Y., Li, D., Liu, Y., & Wang, Z, "A 16-bit high-speed sigma-delta ADC with low-power consumption in 0.18μm CMOS", IEEE Transactions on Circuits and Systems II: Express Briefs, (2022), 69(4), 1123-1127.

[8] Liu, M., Zhang, X., Wang, L., & Li, Y, "A 12-bit low-power sigma-delta ADC with a novel dynamic reference and error feedback loop", IEEE Journal of Solid-State Circuits, (2022), 57(1), 205-216.

[9] Yang, L., Zhang, Y., & Zhang, B, "A 14-bit high-speed sigma-delta ADC with a novel digital correction loop for high-resolution audio applications", IEEE Transactions on Circuits and Systems I, (2021), 68(10), 3457-3466.

[10] Wu, Y., Liu, F., & Wang, Y, "A 10-bit low-power sigma-delta ADC with a novel low-distortion modulator and error feedback loop", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (2021), 29(4), 1141-1150.

[11] Li, B., Zhang, Y., & Wang, Z, "A 10-bit low-power sigma-delta ADC with a novel multi-loop error feedback architecture", IEEE Transactions on Circuits and Systems I, (2020),67(11), 3914- 3923.

[12] Y. Wang, J. Wang, and X. Zhang, "A Low-Power Voltage-to-Current Converter with a Novel Current Mirror," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 12, pp. 3267-3277, Dec. 2020