Comparative Analysis and Experimental Evaluation of 3-Level NPC and Cascaded H-Bridge Inverters for Electric Power Applications

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Abstract

This research paper focuses on the implementation and testing of a three-phase, three-level cascaded H-bridge inverter. The inverter is tested on both a three-phase motor and a resistive load to evaluate its performance and efficiency. The paper also discusses the modulation algorithm used for the two types of inverters, namely the cascaded H-bridge and the multi-structure, using the dSPACE 1104 and Microlabbox. The implementation of the inverter is crucial for various applications, including renewable energy systems and electric vehicles. The testing on a three-phase motor provides insights into the inverter's ability to control the motor's speed and torque accurately. Additionally, the resistive load testing helps assess the inverter's performance under different load conditions. The modulation algorithm applied to the inverters plays a vital role in achieving optimal performance and reducing harmonic distortion. The dSPACE 1104 and Microlabbox are utilized as reliable platforms for implementing and evaluating the modulation algorithm. The results obtained from the testing and implementation of the inverter and modulation algorithm provide valuable information for future research and development in the field of power electronics.

Keywords: -NPC inverter; Cascaded H-bridge inverter; dSPACE 1104; Microlabbox; Three-phase motor.

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1. Introduction

In recent years, the implementation of inverters has gained significant attention in various industries, particularly in the field of power electronics[1]. Inverters play a crucial role in converting direct current (DC) into alternating current (AC), enabling the efficient utilization of electrical energy. Among the different types of inverters, the three-phase 3-level cascaded H-bridge inverter has emerged as a promising solution due to its ability to provide higher voltage levels and improved power quality. This research paper aims to explore the implementation and testing of such an inverter, specifically focusing on its application in different scenarios.The current world is witnessing a significant rise in energy consumption. The utilization of multilevel inverters in

power electronics is a crucial technology. In industrial settings, employing a multilevel inverter for AC drives offers exceptional performance and is the optimal choice for energy conservation [2]. Multilevel inverters utilize medium voltage semiconductor devices and sources to generate high-output power. Medium voltage sources like batteries, super capacitors, and solar panels can be employed. This technology is gaining popularity for large-scale industrial drive applications. In comparison to traditional two-level inverters, multilevel inverters possess numerous advantages. They can produce output voltage waveforms at low switching frequencies, thereby reducing switching losses, enhancing efficiency, minimizing harmonic distortion, and generating nearly sinusoidal output. Furthermore, power switches experience lower voltage stresses and there is reduced electromagnetic interference [3]–[5]. However, the use of multilevel technology necessitates a higher number of switches, which complicates the control circuitry.

The first section of this paper delves into the implementation of the three-phase 3-level cascaded H-bridge inverter. This particular inverter configuration consists of multiple H-bridge modules connected in series, allowing for the generation of three-phase AC output with three voltage levels. The advantages of this configuration include reduced switching losses, improved voltage waveform quality, and enhanced power conversion efficiency. By analyzing the implementation process, this research aims to provide valuable insights into the practical aspects of utilizing this inverter in real-world applications[6].

The second section of this paper focuses on the testing of the three-level inverter, specifically in two different scenarios. Firstly, the inverter's performance is evaluated when connected to a three-phase motor. This test aims to assess the inverter's ability to drive a motor efficiently and reliably. Secondly, the inverter is tested with a resistive load to analyze its performance under different load conditions. By conducting these tests, this research aims to provide a comprehensive understanding of the inverter's capabilities and limitations in various operating conditions.

Furthermore, this research paper presents the modulation algorithm applied to the two 3-level inverters, namely the cascaded H-bridge and Multi-structure inverters, using the dSPACE 1104 and Microlabbox. The modulation algorithm plays a crucial role in controlling the switching patterns of the inverter, ensuring the generation of high-quality AC output. By presenting the modulation algorithm, this research aims to provide a detailed explanation of the control strategy employed in these inverters, enabling researchers and practitioners to replicate and further enhance the performance of these inverters in their own applications[7], [8].

This research paper aims to contribute to the existing knowledge on the implementation and testing of the three-phase 3-level cascaded H-bridge inverter. By exploring the practical aspects of utilizing this inverter in different scenarios and presenting the modulation algorithm employed, this research provides valuable insights for researchers and practitioners in the field of power electronics. The findings of this research can potentially pave the way for the widespread adoption of this inverter configuration, leading to improved power conversion efficiency and enhanced power quality in various industries.

2. Neutral-Point-Clamped (NPC) 3 Level Inverter

2.1 Structure

The three-level NPC inverter is shown in figure 1. The input DC bus is composed of two capacitors in series (C1 and C2), forming a midpoint denoted (o) which allows the inverter to access an additional voltage level compared to the conventional inverter at two levels [9]. The total DC bus voltage is equal to; under normal operating conditions, this is uniformly distributed over the two capacitors which then have a voltage at their terminals.

Each of the three arms (1, 2 and 3) of the inverter consists of four controlled switches (S1, S2, S3 and S4 for arm a) and two holding diodes connected to the midpoint of the DC bus. The controlled switches are unidirectional in voltage and bidirectional in current: they are classic associations of a transistor and an antiparallel diode.

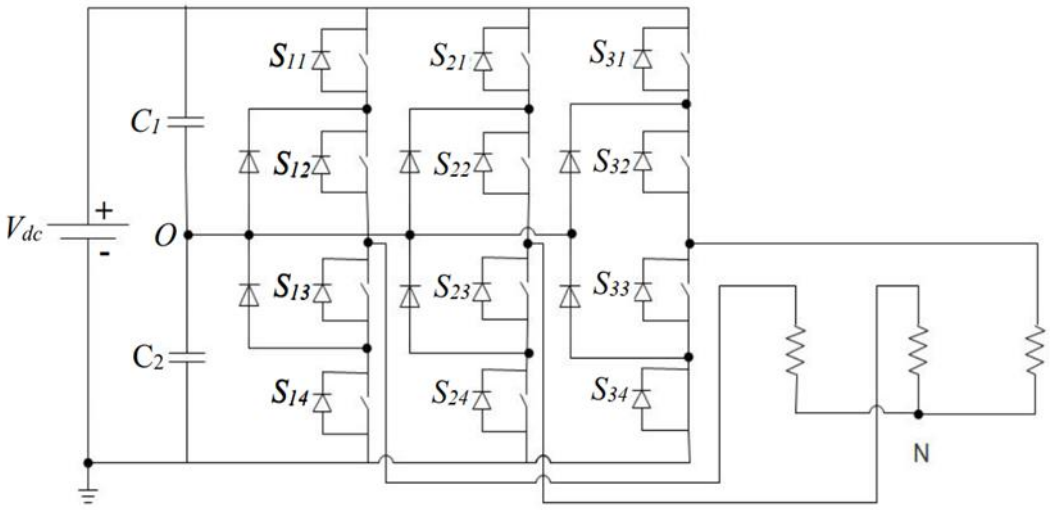

Figure 1: Three-phase NPC 3-level inverter.

2.2 Principle of operation

For sake of simplicity, we will limit the study to a single-phase three-level neutral point clamped (NPC) converter. The aim is to determine the values that the Vao voltage can take for the different possible states of the static switches, as well as to demonstrate the sequences of switch conduction.

The direction of energy transmission from the converter is determined by the positive or negative direction of the currents Ido, Id1 and Id2. The current flow across transistors while the voltage source generates, and the load receives. When energy is transferred from the load to the input source, it is the antiparallel diodes that are responsible for ensuring that the current is passed through the circuit (figure 2).

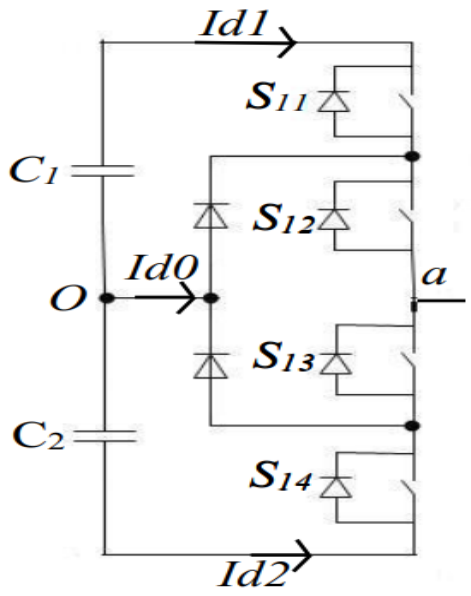

Figure 2: A single-phase three-level neutral point clamped (NPC) inverter.

The NPC converter with N-levels of voltages has N possible sequences of operation which allow it to generate the N levels of voltages. This means that we have N possible sequences of operation for the NPC converter. For the three-level NPC, we have three switching sequences that are possible:

- **Sequence 1: {1100} Generation of the maximum level.**

As illustrated in Figure 3, the switches S1 and S2 are closed (that is ON), whereas the switches S3 and S4 are open (switched OFF). And the output voltage Vao is as follows:

$$Vao = +Vdc/2 \quad (1)$$

The inverse voltage applied to switches S3, S4 is:

$$VS3 = VS4 = +Vdc/2 \quad (2)$$

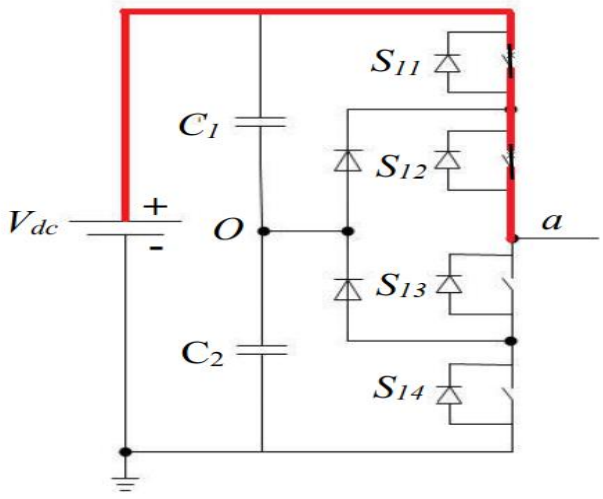

Figure 3: 1st configuration of a single-phase three-level NPC inverter.

- **Sequences 2: {0110} Generation of the intermediate level.**

As illustrated in figure 4, when the switches S2, and S3 are turned on and the switches S1, and S4 are turned OFF, the point a is directly connected to point "O" through one of the maintaining diodes. And as a result, the output voltage Vao is zero:

$$Vao = 0 \tag{3}$$

The reverse voltage that is applied to the switches S1 and S4:

$$VS1 = VS4 = +Vdc/2 \tag{4}$$

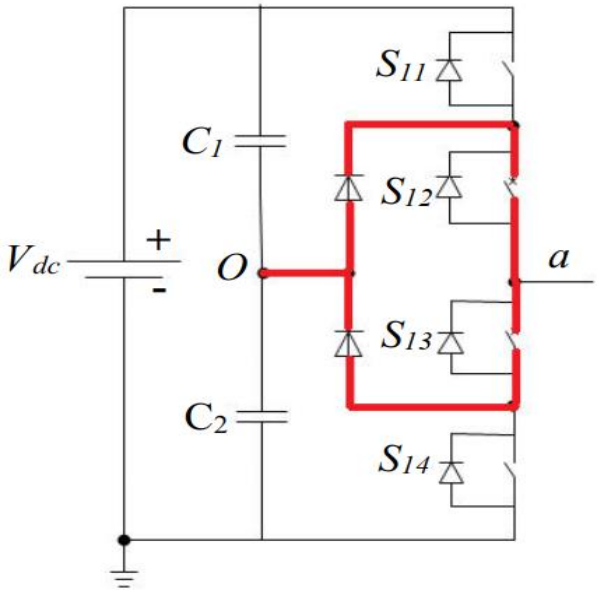

Figure 4: 2nd configuration of a single-phase three-level NPC inverter.

- **Sequences 3: {0011} Generation of the minimum level.**

In this case, the switches S1, and S2 are turned on and S3, and S4 are turned oFF, as shown in figure 5. And the Vao output voltage is:

$$Vao = -Vdc/2 \tag{5}$$

The inverse voltage applied to the switches S1, and S2 is:

$$VS1 = VS2 = +Vdc/2 \tag{6}$$

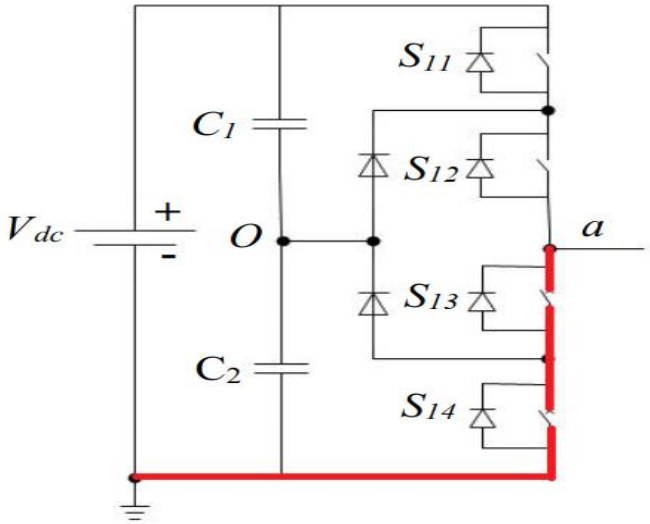

Figure 5: 3rd configuration of a single-phase three-level NPC inverter.

The three possible switching states and the Vao output voltage of a 3-level NPC inverter are summarized in Table1:

Table 1: Switching states of a single-phase 3-level NPC inverter.

Symbol	Device switching states				Terminal voltage Vao
	$S11$	$S12$	$S13$	$S14$	
P	1	1	0	0	$+Vdc/2$
O	0	1	1	0	0
N	0	0	1	1	$-Vdc/2$

The control signals of each switch and the waveform of the output voltage Vao are depicted in figures 6 to illustrate the sequences operation described above.

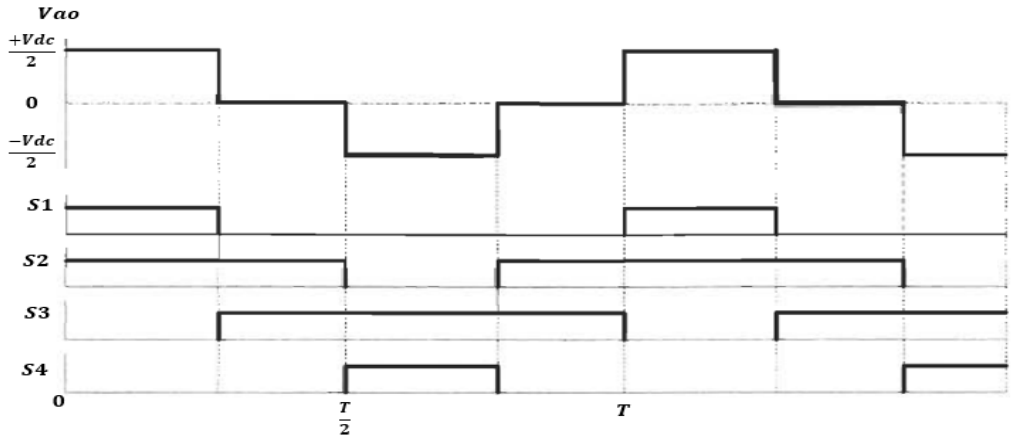

Figure 6: Waveforms of a single phase three-level NPC inverter.

3. Cascaded H-Bridge Three-level Inverter

3.1 Structure

The structure of a three-level converter based on the series connection of three single-phase inverters H-bridge (or partial cell) is shown in figure 7. The structure of a single phase three-level cascaded H-bridge inverter is identical to that of a classic single-phase full-bridge inverter, see figure 8. However, the control technique is different, which will make it possible to have the three voltage levels[10].

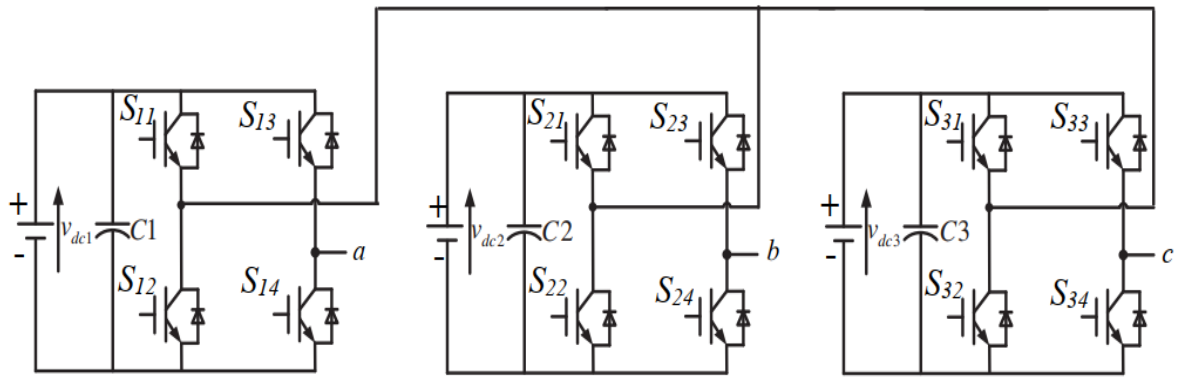

Figure 7: Cascaded H-Bridge Three-level Inverter.

The three cells are star-connected. However, it is also possible to connect them in a triangle [11]. Each cell of the inverter is powered by a DC source E and consists of four switches which are unidirectional in voltage and bidirectional in current, these are conventional combinations of a transistor and a diode in antiparallel. The sources must be galvanically isolated from each other, in order to avoid a short-circuit when they are connected in series[12].

3.2 Principle of operation

In order to have a better understanding of the operation of the cascade structure in an H bridge with three voltage levels, our study will be limited to the single-phase structure shown in figure 8.

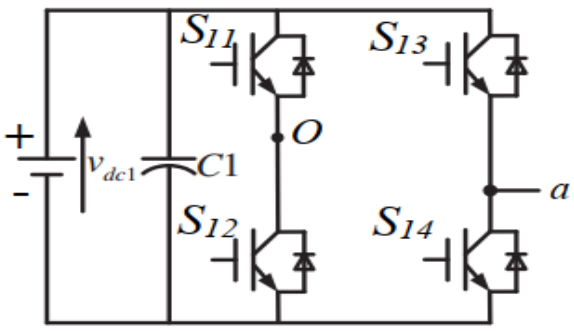

Figure 8: A single-phase three-level cascaded H-bridge inverter.

Therefore, the aim is to determine the values of the output voltage Vao that can be achieved for the different possible states of the switches, as well as to illustrate the conduction sequences of the switches.

Similarly, to the case of the three-level NPC inverter, there are three possible sequences of operation for CHB:

- **Sequence 1: {1001} Generation of the maximum level.**

In this case, switches S1, S4 are on and S2, S3 are blocked as shown in figure 9. And the output voltage Vao is:

$$Voa = +Vdc \quad (7)$$

The reverse voltage applied to switches S2, S3 is:

$$VS2 = VS3 = +Vdc \quad (8)$$

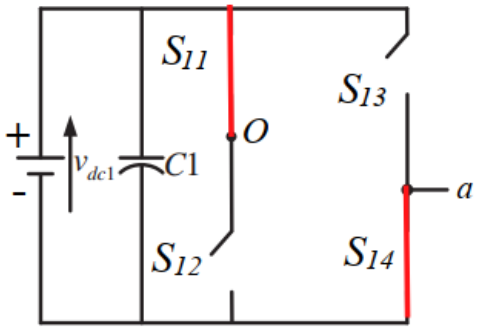

Figure 9: 1st configuration of a single-phase three-level CHB inverter.

- **Sequences 2: {0101} Generation of the intermediate level.**

In this case, the switches S2, S4 are turned on and S1, S3 are blocked, as shown in figure 10. And the Vao output voltage is:

$$Vao = 0 \quad (9)$$

The reverse voltage applied to switches S1, S3 is:

$$VS1 = VS3 = +Vdc \quad (1)$$

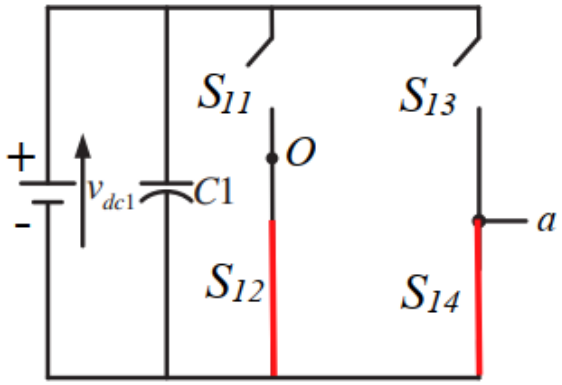

Figure 10: 2nd configuration of a single-phase three-level CHB inverter.

- **Sequences 3: {0110} Generation of the minimum level.**

In this case, the switches S1, S4 are turned off and S2, S3 are turned on, as shown in figure 11. And the Vao output voltage is:

$$Vao = -Vdc \qquad (11)$$

The inverse voltage applied to the switches S1, and S2 is:

$$VS1 = VS4 = +Vdc \qquad (12)$$

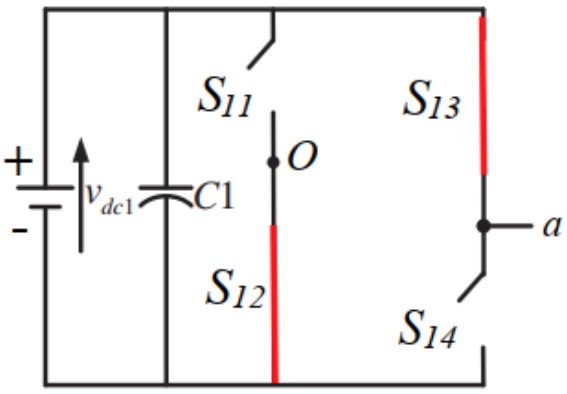

Figure 11: 3rd configuration of a single-phase three-level CHB inverter.

The three possible switching states and the Vao output voltage of a 3-level CHB inverter are summarized in Table 2:

Table 2: Switching states of a single-phase 3-level CHB inverter.

Switching states	Device switching states				Terminal voltage Vao
	$S11$	$S12$	$S13$	$S14$	
P	1	0	0	1	$+Vdc$

O	0	1	0	1	0
N	0	1	1	0	$-Vdc$

The operation sequences, output voltage waveform and switch states are shown in figure 12:

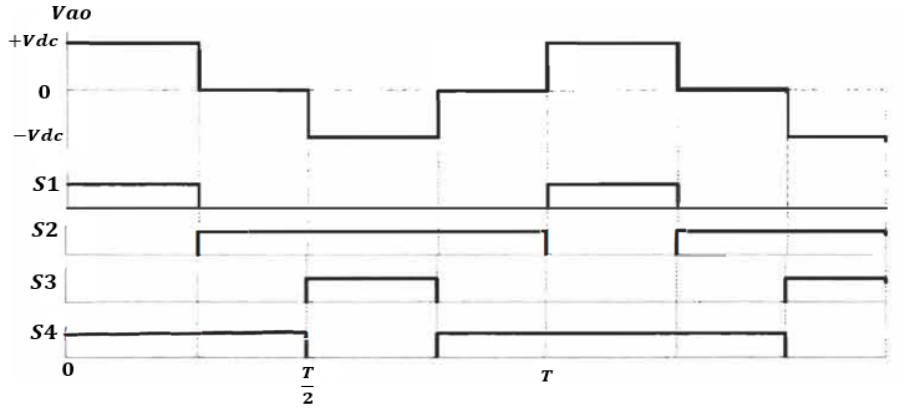

Figure 12: Waveforms of a single phase three-level CHB inverter.

Consider that the conduction time of each switch is the same as that of the switches of a single-phase three-level NPC inverter. The further important point is that with each change in voltage level, a single switch (IGBT) changes its state, so the switching losses are significantly reduced.

4. Result and Discussion

Figure 13 and Table 3 show the different parts making up our final prototype, namely: The control (dSPACE 1104, the control-power interface part, the power part, the current and voltage measurement part (sensor) as well as the digital oscilloscope.

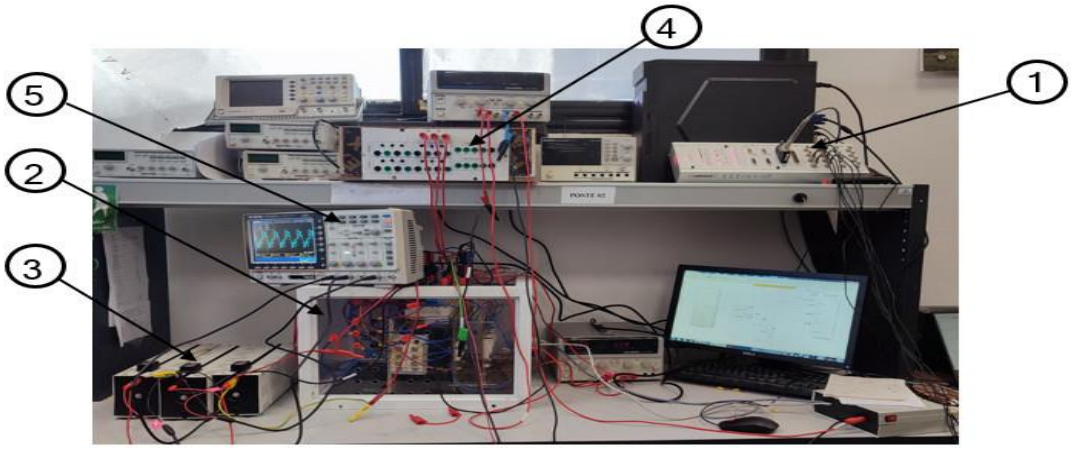

Figure 13: Different parts constituting the prototype of a three-level inverter.

Table 1 : Different parts constituting the prototype of the inverter has three levels.

NUMBER	COMPONENTS
1	dSPACE 1104
2	CHB-Inverter
3	Load
4	Sensor
5	Oscilloscope

The 3-level h-bridge inverter is defined in Table 4 by the following characteristics:

Table 4: Characteristics of the prototype 3-level Cascaded H-Bridge Inverter.

Magnitude	Value
The transferred power **P**	180/90 W
DC input voltage **Vdc**	120/60 V
Rated current **In**	1.5/ A
Output rms voltage (Star) **V**	120 V
Switching frequency **fS**	2.5-5 kHz

4.1 Generation of Dead Time:

The creation of dead time makes it possible to avoid short-circuit problems linked to the opening and closing time of the switches, since the IGBTs have a firing time much lower than the blocking time and the switching cells are complementary [13].

If one IGBT is turned on, the other IGBT of a half bridge cannot be switched. Additionally, a digitally adjustable interlocking time is generated by the driver SKHI 22A, which has to be longer than the turn-off delay time of the IGBT. This is to avoid that one IGBT is turned on before the other one is not completely discharged. The interlocking time of the driver SKHI 22A stages in

half bridge applications is adjusted to 3,25 µs. It may be increased up to 4,25 µs by applying a 15 V (VS) supply voltage at Pin 9 (TDT2) (Figure 14) [14].

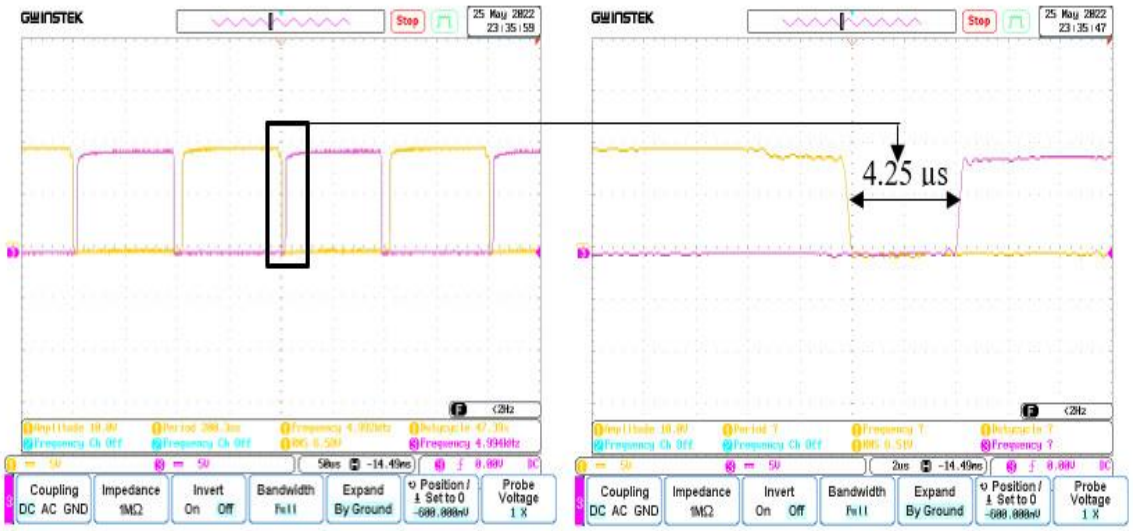

Figure 14:Control signals for the 3-level cascaded H bridge inverter with dead time generation of 4.25 µs.

4.2 The Implementation of Modulation Strategies of the 3 Level H-Bridge Inverter:

Figure 15 presents the control signals for the unipolar PWM control such that chains 1, 2, 3 and 4 present the control of the switches S11, S12, S13, and S14, respectively. for r=1 and fs=2.5KHz.

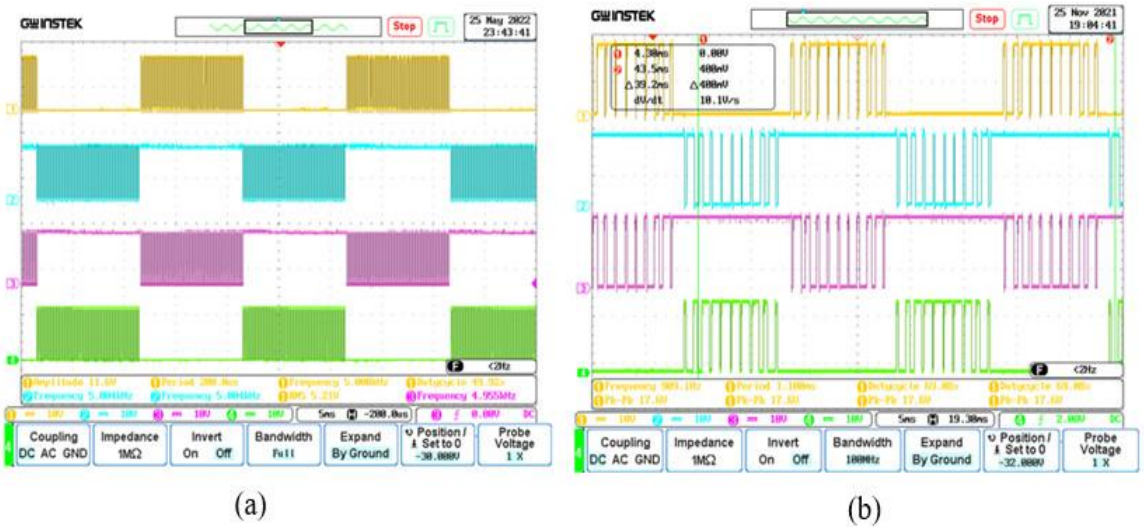

Figure IV 15: Unipolar PWM control signals: (a) for 5 kHz, (b) for 2.5 kHz.

4.3 CHB 3-Level Inverter with Resistive Load:

In Figure 16, the unipolar PWM implementation is depicted with specific parameters. The sampling frequency is set at 2.5 kHz, while the value of r is 1. The reference frequency is 50 Hz, and the DC bus voltage is 60 V.

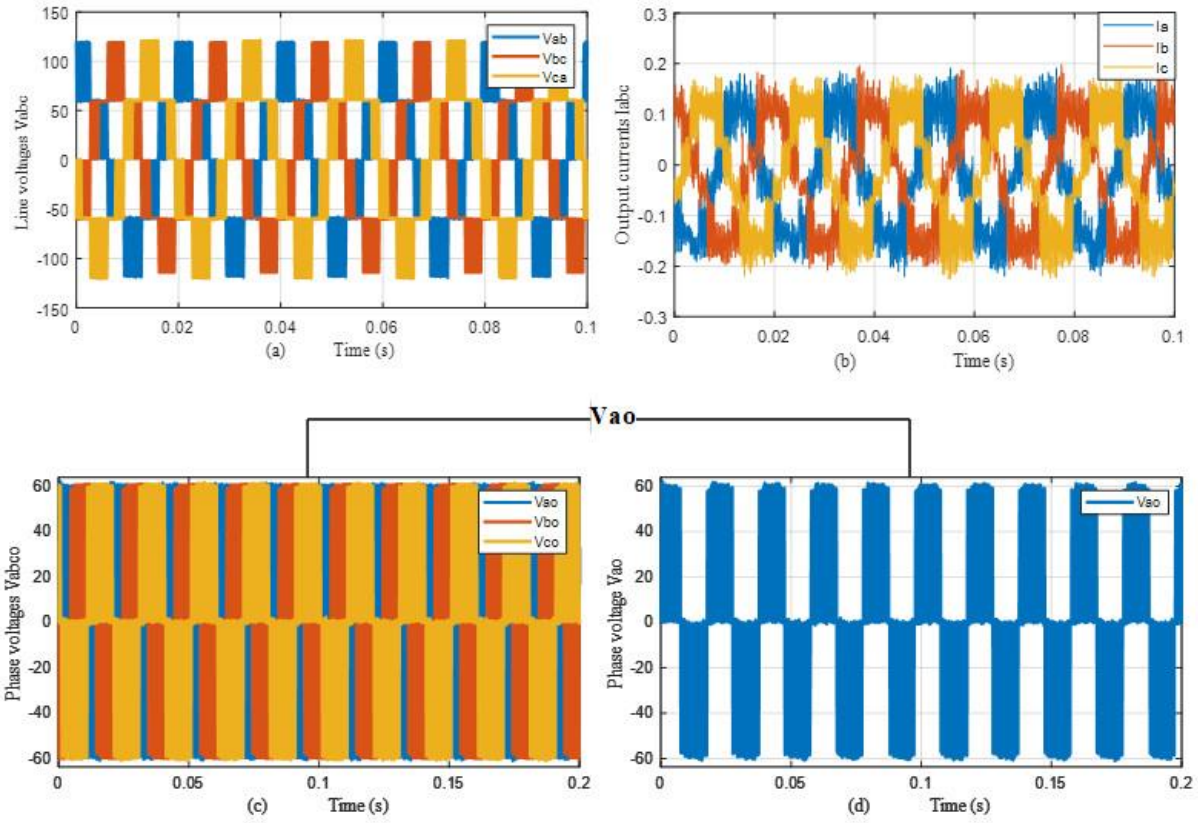

Figure 16: Inverter output voltage and current for resistive load (R=23): (a) The output line voltage waveform Vabc, (b) Load currents 'iabc', (c) Phase voltages Vabco, (b) Vao phase voltage.

In Figure 16 (a), it can be observed that the experimental and simulated line voltages have the same number of levels, indicating similarity between the two.Moving on to Figure 16 (b), it is evident that the current measurement, represented as a wave, has undergone deformation due to the lack of filtering.

Figures 16 (c) and (d) further support the similarity between experimental and simulated results, as the phase voltages obtained show a similar pattern.

4.4 CHB 3-Level Inverter with Three-Phase Motor:

Figures 17 and 18 illustrate the application of a three-level inverter on a three-phase motor. The implementation involves a sampling frequency of 5 kHz using unipolar PWM, a reference frequency of 50Hz, and a DC bus voltage of 80V for each cell.

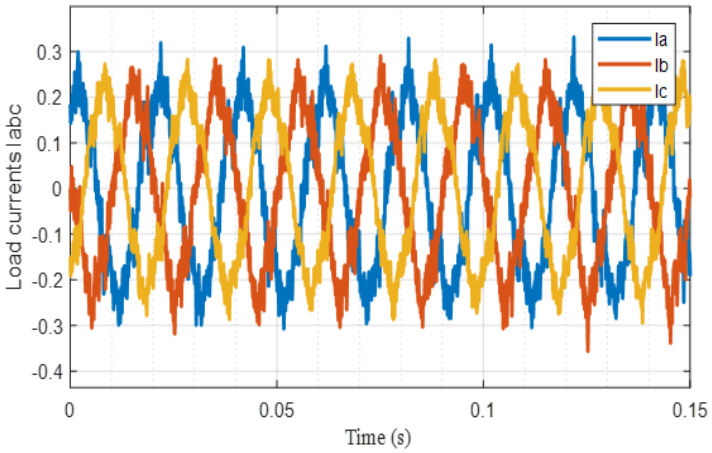

Figure 17: Three-phase motor currents *iabc*.

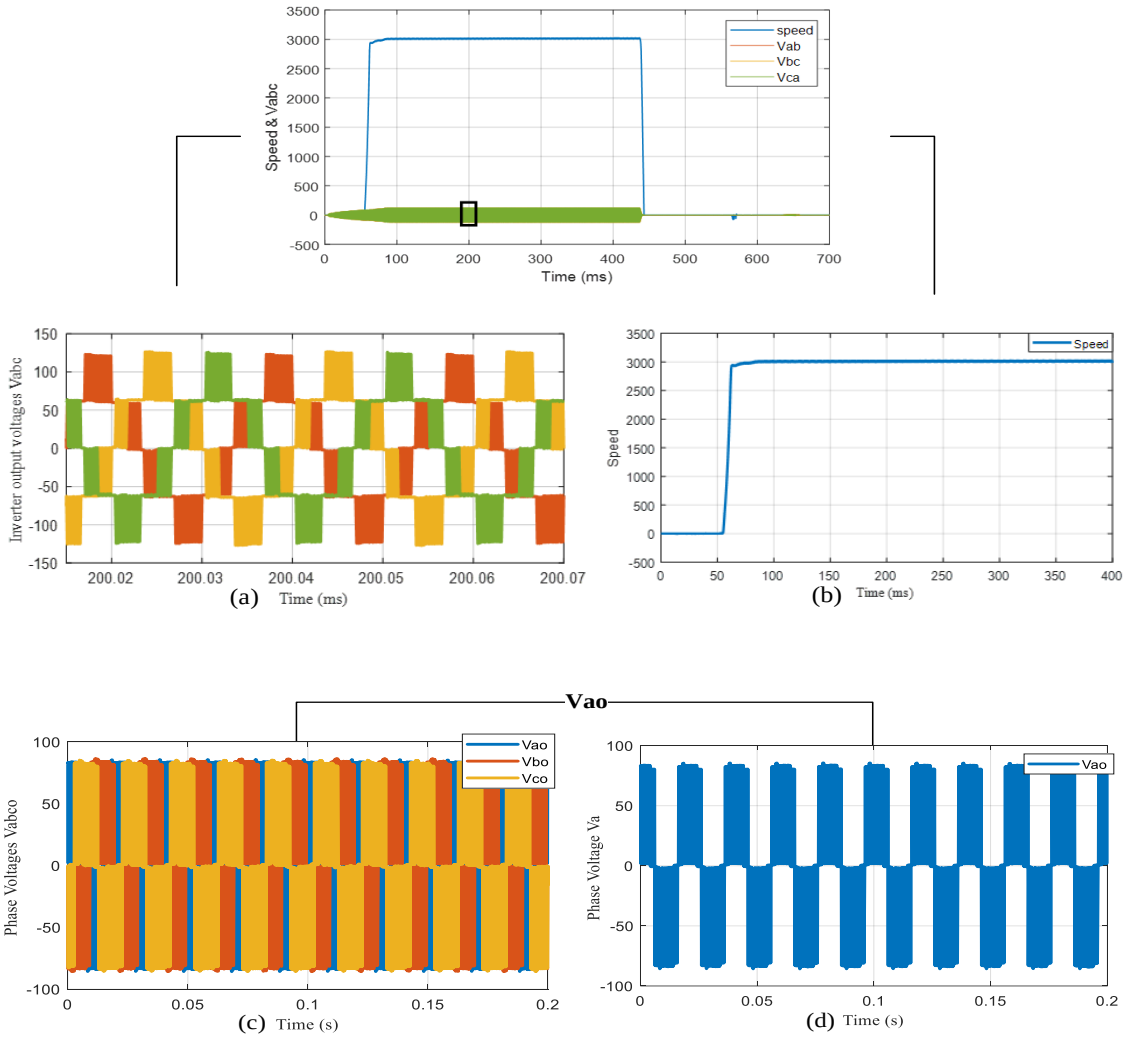

Figure 18: Experimental results for unipolar PWM with r=1 and fs=5kHz: (a) The motor line voltage waveform Vabc, (b) Motor speed, (c) Phase voltages Vabco, (b) Vao phase voltage.

Figures 17 and 18 depict the currents of a three-phase motor, the line voltage of the motor, and the motor speed. The cascade inverters used in this scenario have a switching frequency of 5kHz and a DC link voltage of 80V. The output frequency is set to 50Hz, resulting in a motor speed of 300rpm. The modulation index is set at 0.9.

5. Conclusion

In conclusion, this research paper focused on the implementation and testing of a three-phase 3-level cascaded H-bridge inverter. The inverter was tested on both a three-phase motor and a resistive load to evaluate its performance and efficiency. The modulation algorithm used for both the cascaded H-bridge and multi-structure inverters was applied using the dSPACE 1104 and Microlabbox. The results obtained from the testing showed that the cascaded H-bridge inverter performed effectively, providing stable and reliable power output to the motor and resistive load. The modulation algorithm implemented through the dSPACE 1104 and Microlabbox proved to be efficient in controlling the inverter and ensuring optimal power conversion. Overall, this research paper contributes to the understanding and advancement of three-level inverters, particularly the cascaded H-bridge design, and provides valuable insights into their implementation and testing. Further research can be conducted to explore the performance of the inverter under different load conditions and to optimize the modulation algorithm for enhanced efficiency and power quality.

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